Comparison of Coplanar 60-GHz Low-Noise Amplifiers Based on a GaAs PM-HEMT Technology

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***Abstract*—For use in low-noise receivers of communication or radar systems, three different two-stage amplifiers for 60 GHz, using a 0.15-μm PM-HEMT technology on GaAs, have been compared in terms of gain and noise figure. The amplifiers realized in coplanar waveguide technology (CPW) differ in the matching networks of the two stages, optimized either for low-noise or maximum gain bias condition. At 59 GHz, a minimum noise figure of 3.0 dB with an associated gain of 9.3 dB and a maximum gain of 12.2 dB with a noise figure of 3.8 dB were achieved.**

***Index Terms*—Coplanar waveguide, low-noise receiver, MMIC amplifier, PM-HEMT.**

I. Introduction

LOW-NOISE amplifiers (LNA's) are essential elements in any communication system front end in wireless LAN's, satellite links, and radiometric sensors. With a 0.3-μm PM-HEMT technology on GaAs, at 60 GHz a noise figure of 5.8 and an associated gain of 9 dB, respectively, were achieved [1], and 4.8 and 12.5 dB were achieved, respectively, for devices with a gate length of 0.18 μm [2]. Using a 0.25-μm InP-based HEMT technology, 2-stage amplifiers with a high gain of 15.2 dB were fabricated [3], and by further reducing the gate length to 0.1 μm, a noise figure of 2.2 dB with a gain of 13 dB was achieved between 56 and 61 GHz [4]. Whereas InP-based monolithic microwave integrated circuits (MMIC's) have shown better performance due to the higher electron mobility, today the higher maturity of GaAs-based PM-HEMT processes yields superior reliability, lower costs, and higher reproducibility of the devices for V-band applications.

Based on our 0.15-μm PM-HEMT process on 3-in GaAs substrates [5] and taking advantage of CPW technology, we compare the achievable performances in terms of noise figure and gain of monolithic 2-stage coplanar amplifiers at V-band with different design approaches with respect to matching networks and device geometry.

II. Circuit Design

For LNA's, there are three main approaches in designing the matching networks: 1) a minimum noise figure limited by the characteristics of the active device can be achieved with matching both stages for low-noise bias condition, at the expense of lower associated gain; 2) optimum gain can be obtained if both stages are properly designed for maximum gain, resulting in a higher noise figure; and 3) a tradeoff between gain and noise performance is made by optimizing the first stage for low-noise and the second for maximum gain bias condition.

Following these approaches, the amplifiers are designed using small-signal simulations. For different bias conditions of the FET, the elements of the small-signal equivalent circuit are extracted from on-wafer S-parameter measurements up to 120 GHz [6]. The noise characteristics of the device are simulated by use of the temperature noise model of Pospiezalski, assigning the ambient temperature to the gate resistance and an elevated equivalent temperature T_d to the output conductance [7]. Depending on the low-noise (LN) or maximum gain (MG) bias condition, the PM-HEMT used for the designs shows the following properties: on the one hand, for a drain current between 100 and 150 mA/mm at $V_{ds} = 1.5$ V—a typical bias condition for low noise—the FET has an intrinsic transconductance of 800 mS/mm and exhibits a current gain cutoff frequency f_T and maximum oscillation frequency $f_{\max}$ of 125 and 220 GHz, respectively, as can be seen in Fig. 1. The value of T_d is 2000K. The noise figure of the device is reduced by optimizing the unit gate width w_g and the number of gate fingers. Thus, for a two-finger device with a unit gate width of 30 μm, a minimum noise figure of 2.3 dB can be obtained at 60 GHz, with a maximum stable gain (MSG) of 8.0 dB. On the other hand, for a drain current between 250 and 300 mA/mm at $V_{\rm ds} = 2$ V, where the HEMT exhibits its maximum intrinsic transconductance of 1150 mS/mm, the transistor shows cutoff frequencies f_T and $f_{\max}$ of 100 and 210 GHz, respectively, and a MSG of 8.9 dB at 60 GHz (Fig. 1). The high drain temperature of 4000K obviously results in an increased noise figure.

Coplanar waveguide technology is chosen for the passive circuitry because of its attractive better characteristics at millimeter-wave frequencies, its low dispersion, low radiation losses, and the ease of connecting both series and parallel circuit lumped elements with relatively low parasitic effects. As an example, the chip photograph of one LNA is shown on Fig. 2. CPW transmission lines, MIM capacitors, NiCr thin film resistors, and air bridges are used for the realization of small-size low-loss matching networks and bias supply. For the transmission lines (having a ground-to-ground spacing of 50 μm), only three central conductor widths are chosen, resulting in characteristic impedances of approximately 30, 50, and 70 Ω. Frequency-dependent models have been developed

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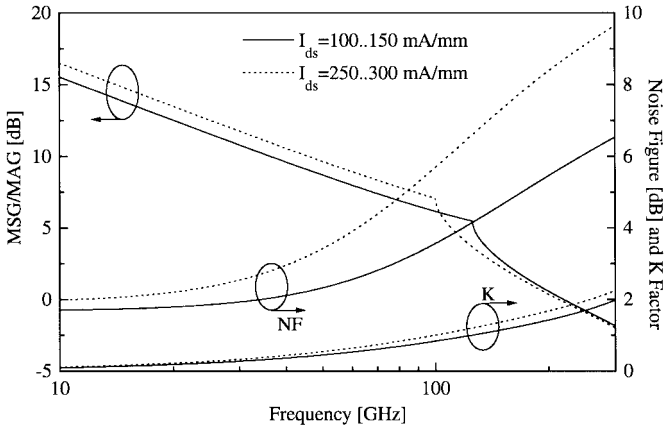

Fig. 1. Simulated MSG/MAG, K factor, and noise figure of the 0.15 × 60-μm PM-MODFET for low-noise and maximum gain bias conditions.

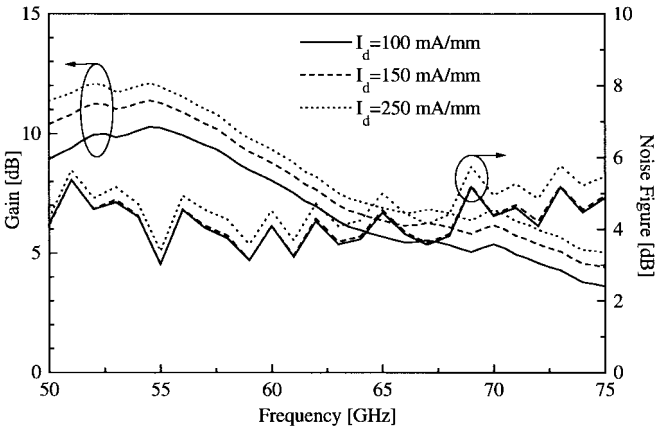

Fig. 3. Measured gain ($|S_{21}|$) and noise figure of the LN/LN amplifier (LNA1) as a function of the bias.

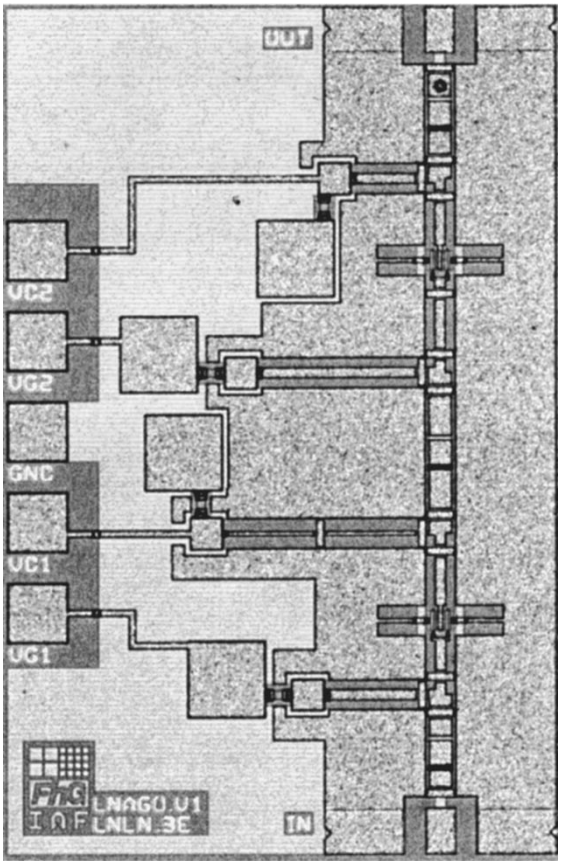

Fig. 2. Chip photograph of the 2-stage LNA (LNA1). Chip size is 1.5 × 1.0 mm^2.

from theoretical properties and on-wafer measurements up to 120 GHz for various building blocks, such as the CPW lines, T-junctions, 90°-bends, probing pads [8], and air bridges [9].

As shown in Fig. 2, for the stabilization of the device at 60 GHz, an inductive feedback on each source pad is realized by a transmission line of 60-μm length. The matching networks of the three different designs are optimized for minimum noise figure (LNA1), for minimum noise figure with optimum associated gain (LNA2), and for maximum gain (LNA3). Thus, both LNA1 stages are operated at low-noise bias condition. In the case of LNA2, the first stage is biased for low noise and the second at maximum transconductance of the FET. The two stages of LNA3 are both biased for maximum transconductance. Consequently, for each stage biased for adequate operation (i.e., low-noise or peak transconductance), the optimum input impedance is determined to give either minimum noise figure or maximum gain. The output impedance is chosen to give the maximum output power transfer. Afterwards, the two stages are cascaded and matched with a direct impedance transformation. A final optimization is performed on the interstage matching network to compensate for the feedback in the active devices.

For LNA1, an improvement of noise figure by use of lower loss interconnections is also investigated. With an air bridge technology using two metallization levels of different thickness, T-junctions are usually realized with the center conductor passing under the ground air bridge connection, exhibiting higher series losses because of the thinner metallization used for signal path. From the simulation, the resulting high series resistance in the input matching stage has a contribution to the noise figure in the order of 0.3 dB. Hence, in a second design (LNA1b), this thin metallization has been used only to connect the ground planes, whereas the radio frequency (RF) power is transmitted via the thick metallization level, providing less series losses.

III. Measured Performance

The amplifiers were measured up to 78.5 GHz with a full two-port corrected S-parameter measurement system and by placing the unthinned wafer (635 μm) directly on a metal chuck. Stable and reproducible noise figure data were determined by means of the 50-Ω hot–cold measurement setup described in [1]. For the three LNA's, the measured performance is depicted in Figs. 3–6. Good agreement between measured and simulated S-parameters was achieved from 0.5 to 78.5 GHz. It has to be mentioned that all amplifiers are absolutely stable over the entire frequency range and that the reverse isolation (S_{12}) is better than 23 dB. In Fig. 3 the amplifier performance of LNA1 is depicted as a function of bias. For a drain current of 100 mA/mm (low-noise bias), the LNA1 has a gain better than 8.5 dB at 59 GHz and a minimum noise figure of 3.1 dB. As shown in Figs. 3 and 4, for $I_d = 150$ mA/mm the gain is increased to 9.2 dB without

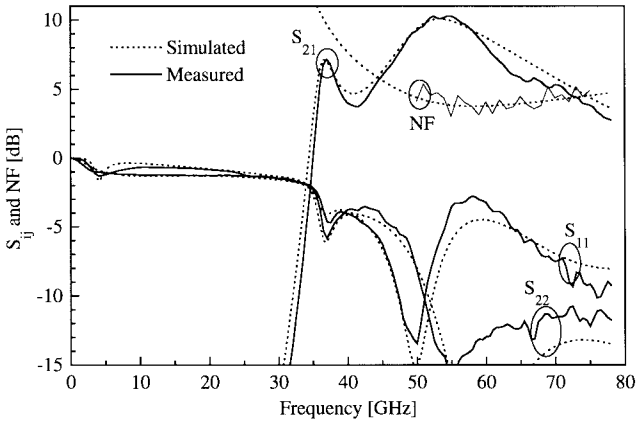

Fig. 4. Measured and simulated S-parameters and noise figure of the LN/LN amplifier (LNA1).

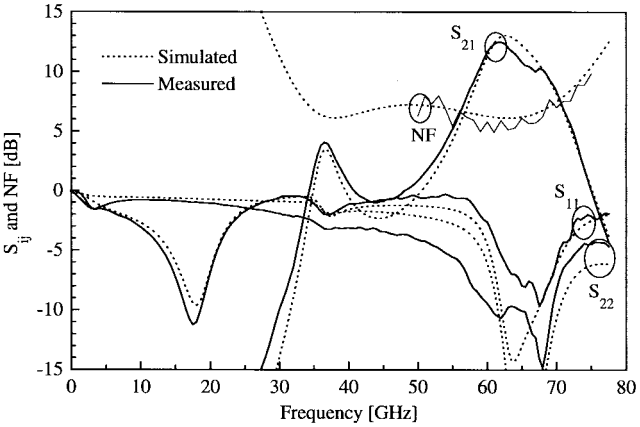

Fig. 5. Measured and simulated S-parameters and noise figure of the MG/MG amplifier (LNA3).

degrading the noise figure. As previously discussed, the use of low-loss T-junctions (LNA1b) results in a slightly lower noise figure of 3.0 dB with a higher associated gain of 9.3 dB (at $I_d = 100$ mA/mm). These values agree well with [10] (0.15-μm GaAs PM-HEMT), where a noise figure of 1.4 dB was measured at 30 GHz, resulting in an estimated noise figure of 2.8 dB at 60 GHz, and are still attractive compared to those achieved with more complex device technologies (0.1-μm InP-based technology, [4]). As can be seen from Fig. 5, the LNA3 shows a reasonable noise figure of 5.9 dB, in good agreement with the predicted results. This design should give the maximum gain of 13.2 dB at 62 GHz. The gain is slightly lower, however, than predicted. Finally, the optimum tradeoff between noise figure and gain is obtained with the design LNA2, where a noise figure and a gain of 3.8 and 12.2 dB were achieved at 59 GHz, as can be seen in Fig. 6.

IV. Conclusion

Three coplanar designs of 60-GHz 2-stage LNA's on a GaAs based 0.15-μm PM-HEMT technology are compared. The achievable noise figure and gain performance is presented for three different approaches regarding transistor (bias and size) and matching network optimizations: The realized LNA's with noise figure/associated gain at 59 GHz of 3.0/9.2 and

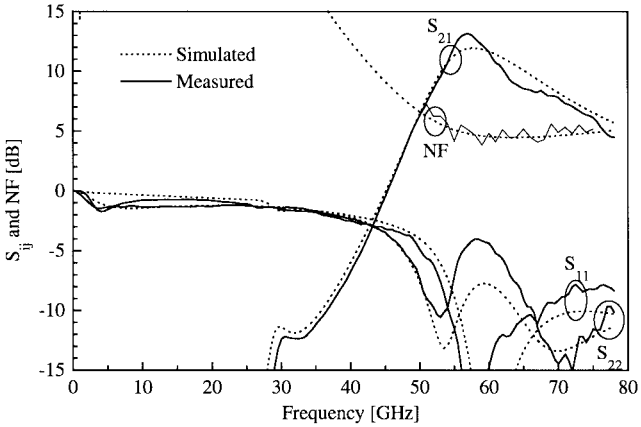

Fig. 6. Measured and simulated S-parameters and noise figure of the LN/MG amplifier (LNA2).

3.8/12.2 dB, respectively, exhibit state-of-the-art performance for a GaAs-based PM-HEMT technology.

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References

[1] M. Schlechtweg, W. Reinert, P. J. Tasker, R. Bosch, J. Braunstein, A. Hülsmann, and K. Köhler, "Design and characterization of high performance 60 GHz pseudomorphic MODFET LNA's in CPW-technology based on accurate S-parameter and noise models," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2445–2451, Dec. 1992.

[2] J. Mizoe, T. Matsumura, K. Unosawa, Y. Akiba, K. Nagai, H. Sato, T. Saryo, and T. Inoue, "A V-band GaAs MMIC chip set on a highly reliable Wsi/Au refractory gate process," in *IEEE Microwave Theory Tech. Symp. Dig.*, 1997, pp. 247–250.

[3] M. Berg, J. Dickmann, R. Guehl, and W. Bischof, "60 and 77 GHz monolithic amplifiers utilizing InP-based HEMT's and coplanar waveguides," *Microwave Opt. Technol. Lett.*, vol. 3, pp. 139–145, Feb. 1996.

[4] L. Tran, R. Isobe, M. Delaney, R. Rhodes, D. Jang, J. Brown, L. Nguyen, M. Le, M. Thompson, and T. Liu, "High performance, high yield millimeter-wave MMIC using InP HEMT's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1996, pp. 9–12.

[5] T. Jakobus, W. Bronner, T. Fink, K. Glorer, J. Hornung, A. Hülsmann, K. Köhler, Z. Lao, B. Raynor, M. Schlechtweg, A. Thiede, and L. Verweyen, "E-beam T-gate technology for pseudomorphic HEMT's on 3′′-GaAs with gate length of 0.15 μm," in *Int. Conf. Gallium–Arsenide Manufacturing Technology Dig.*, Seattle, WA, 1998.

[6] M. Schlechtweg, W. H. Haydl, A. Bangert, J. Braunstein, P. J. Tasker, L. Verweyen, H. Massler, W. Bronner, A. Hülsmann, and K. Köhler, "Coplanar millimeter-wave IC's for W-band applications using 0.15 μm pseudomorphic MODFET's," *IEEE Trans. Microwave Theory Tech.*, vol. 31, pp. 1426–1433, Oct. 1996.

[7] M. W. Pospiezalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, Dec. 1989.

[8] W. H. Haydl, A. Tessmann, K. Züfle, H. Massler, T. Krems, L. Verweyen, and J. Schneider, "Models of coplanar lines and elements over the frequency range 0–120 GHz," in *26th European Microwave Conf.*, 1996, pp. 996–1000.

[9] A. Bessemoulin, C. Algani, G. Alquié, and V. Fouad-Hanna, "A simple airbridge analytical model in coplanar waveguides for MMIC applications," *Microwave Opt. Technol. Lett.*, vol. 17, pp. 265–267, Mar. 1998.

[10] S. Fujimoto, T. Katoh, T. Ishida, T. Oku, Y. Sasaki, T. Ishikawa, and Y. Mitsuri, "Ka-band ultra low noise MMIC amplifier using pseudomorphic HEMT's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Denver, CO, 1997, pp. 17–20.